

CLAIMS

1. An automatic decoding method for mapping and selecting a non-volatile memory device having a LPC serial communication interface, wherein the memory is equipped with a plurality of addressing pins and mounted on a motherboard together with other memories of the same type bidirectionally connected with a controller putting it into communication with a processor housed in turn on the motherboard, comprising:

a processor that compares the addressing pins of each memory with a portion of the addressing coding bits both to identify the addressing type to be used, top-down or bottom-up, and to determine which memory is polled by the controller for a given operation.

2. A method according to claim 1, wherein the comparison is performed in a LPC decoding block.

3. A method according to claim 2, wherein the addressing coding is a thirty-two-bit coding and the most significant bits $A<31:25>$ are used to identify the addressing type, while some intermediate bits $A<24:21>$ are used for being compared with the addressing pins to determine which memory is polled by the controller.

4. A method according to claim 3, wherein the most significant bits $A<31:25>$ are processed in a selecting block in the LPC decoding to generate respective identification signals of the addressing type.

5. A method according to claim 4, wherein some intermediate bits $A<24:21>$ are compared with the pins in a comparator block of said LPC decoding driven by an enabling signal generated by a generator block which receives at its input identification signals of the addressing type.

6. A method according to claim 5, wherein the generator block is enabled by a signal outputted by a register incorporating a CAM structure.

7. A non-volatile memory integrated device equipped with an interface with LPC serial protocol and a plurality of addressing pins in order to be mounted on a motherboard together with other memories of the same type bidirectionally connected with a controller putting it into communication with a processor housed in turn on the motherboard, wherein:

the processor contains in the LPC interface a logic identification structure both of the memory and of the addressing type to be used, top-down or bottom-up; and

the logic structure contains a comparator to compare a portion of the addressing coding bits with the addressing pins.

8. A device according to claim 7, wherein the addressing coding is a thirty-two-bit coding and the most significant bits A<31:25> are processed in a selector to generate respective identification signals of the addressing type, while some intermediate coding bits A<24:21> are compared in the comparator with the addressing pins to determine which memory is polled by the controller.

9. A device according to claim 8, wherein the comparison in the comparator is driven by an enabling signal generated by a generator block which receives at its input said identification signals of the addressing type.

10. A device according to claim 9, wherein the generator block is enabled by a signal outputted by a register incorporating a CAM structure.

11. A method for a memory selecting scheme in which a plurality of memory circuits exist, comprising:

reading identification signals indicating whether a top-down or bottom-up decoding scheme is used; and

selecting a particular memory circuit by matching the identification signals to addressing pins on the memory circuit.

12. The method of claim 11 further comprising the step of sending a reset pulse if the identification signals do not indicate a unique decoding scheme.

13. The method of claim 11 further comprising the step of sending a reset pulse if there is not a direct match between the enabling signal and the bits residing on addressing pins of the memory circuit.

14. A nonvolatile memory device for enabling decoding logic, comprising:

a plurality of FLASH memory cells connected in parallel to read identification signals indicating what decoding scheme is used;

a FLASH memory cell sharing a source and gate with the FLASH memory cells used to read, with the function of writing the identification signal to the inverter latch; and

an inverter latch to enable the decoding logic, if a unique decoding scheme is specified and the identification signal matches the addressing bits of the memory.

15. The device according to claim 14 wherein the nonvolatile memory device is a register incorporating a CAM structure.

16. The device according to claim 14 further comprising a bias circuit to bring the voltage on the output of the inverter latch up to a minimum level.